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INFORMATION DISCLOSURE STATEMENT BY APPLICANT		APPLICANT: S. Babar Raza et al.				
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U.S. PATENT DOCUMENTS						
Examiner Initial	Document No.	Date	Name	Class	Sub-Class	Filing Date
FOREIGN PATENT DOCUMENTS						
	Document No.	Date	Country	Class	Sub-Class	Transl.
						Yes
						No
OTHER DOCUMENTS (Incl. Author, Title, Date, Pertinent Pages, etc.)						
	S. Babar Raza et al., "ARCHITECTURE FOR IMPLEMENTING VIRTUAL MULTIQUEUE FIFO", U.S. Serial No. 09/676,704, Filed September 29, 2000.					
	S. Babar Raza, et al., "LOGIC FOR PROVIDING ARBITRATION FOR SYNCHRONOUS DUAL-PORT MEMORY", U.S. Serial No. 09/676,169, Filed September 29, 2000.					
	S. Babar Raza et al., "LOGIC FOR INITIALIZING THE DEPTH OF THE QUEUE POINTER MEMORY", U.S. Serial No. 09/676,705, Filed September 29, 2000.					
	S. Babar Raza et al., "METHOD AND LOGIC FOR INITIALIZING THE FORWARD-POINTER MEMORY DURING NORMAL OPERATION OF THE DEVICE AS A BACKGROUND PROCESS", U.S. Serial No. 09/676,170, Filed September 29, 2000.					
	S. Babar Raza et al., "METHOD FOR LOGIC FOR STORING AND EXTRACTING IN-BAND MULTICAST PORT INFORMATION STORED ALONG WITH THE DATA IN A SINGLE MEMORY WITHOUT MEMORY READ CYCLE OVERHEAD", U.S. Serial No. 09/676,171, Filed September 29, 2000.					
Examiner	<i>[Signature]</i>		Date Considered	9/16/04		